PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Ryo KUBOTO, et al.

Docket No: Q62494

Appln. No.: 09/817,233

Group Art Unit: 2823

Confirmation No.: 8072

Examiner: Hsien Ming LEE

Filed: March 27, 2001

For: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE HAVING DRAM CAPACITORS

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

1. Japanese Unexamined Patent Application Publication No. H11-261021, published September 24, 1999 (corresponding to U.S. Patent No. 6,387,744).
2. Japanese Unexamined Patent Application Publication No. 2000-082803, published May 21, 2000.
3. Japanese Unexamined Patent Application Publication No. H11-186524, published July 9, 1999 (previously submitted on December 4, 2002).

4. Japanese Unexamined Patent Application Publication No. H11-307740, published November 5, 1999 (previously submitted on December 4, 2002)
5. Japanese Unexamined Patent Application Publication No. H07-066295, published March 10, 1995 (previously submitted on December 4, 2002).

One copy of each of the listed documents is submitted herewith, except those listed as previously submitted.

The present Information Disclosure Statement is being filed after the later of three months from the application's filing date and the mailing date of the first Office Action on the merits, but before a Final Office Action, Notice of Allowance, or an action that otherwise closes prosecution in the application (whichever is earlier), and therefore Applicant is filing concurrently herewith a Statement Under 37 C.F.R. § 1.97(e). No fee under 37 C.F.R. § 1.17(p) is required.

In compliance with the concise explanation requirement under 37 C.F.R. § 1.98(a)(3) for foreign language documents, Applicant encloses here with a copy of a corresponding Japanese Office Action dated August 13, 2003 and an English translation of the pertinent portions thereof which cites such documents and indicates the degree of relevance found by the foreign office.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

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Registration No. 22,775

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WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: November 13, 2003

Dispatch Date: 8/13/2003

Q62494

Note (For a list of the cited literature, see the List of Cited Literature.)

(Claims 1 through 7)

- Reasons 1
- Cited Literature, etc. 1–5
- Remarks

Cited Literature 1 describes a manufacturing method for a semiconductor laminated circuit device wherein a DRAM memory cell field having a cylindrical-shaped lower capacity electrode, a DRAM peripheral circuit field, and a CMOS logic circuit field are mounted on a semiconductor substrate (in particular, refer to Figure 31). Cited Literature 2 describes a manufacturing method for a semiconductor device that is comprised of a memory cell having a stack-type capacitor and a peripheral/logic circuit, wherein a polycrystal silicon film is formed on the interlayer insulation of the memory cell and the peripheral/logic circuit, a thermal process is carried out in a designated atmosphere, and boron is injected into the polysilicon gate electrode of a p-channel transistor in the logic circuit. (In particular, refer to Figures 2 and 3). Cited Literature 3 describes a manufacturing method for a semiconductor that is comprised of a peripheral circuit and a memory cell, wherein an interlayer insulation film is formed on the peripheral circuit and memory cell, an opening is formed on the interlayer insulation film on the memory cell, a polysilicon film is formed on the inside of the opening and on the entire surface of said interlayer insulation film, a seed crystal is formed on the surface of the polysilicon film, dry etching is carried out using a resist as a mask, and the cylindrical-shaped lower electrode of the capacitor is formed at the opening (in particular, refer to Figures 21 to 24). There is no particular reason to limit the area of the polysilicon film formation to the area of the peripheral circuit as described in Cited Literature 3; and as described in Cited Literature 2, when a logic circuit is consolidated, it is preferable to form a polysilicon film on the entire surface of the memory cell and the peripheral/logic circuit rather than selectively forming a polysilicon film. Cited Literature 4 states that BPSG film is employed as an interlayer insulation film in which an opening is formed on the cylinder (in particular, refer to Figure 7). Cited Literature 5 describes a CMOS provided in a peripheral field wherein n+polysilicon is employed as the gate electrode of a p-channel transistor (in particular, refer to Figure 1). Phosphorus is well known as an n-type impurity, so a person skilled in the art could have naturally arrived at the inventions in Claims 1 through 7 of the present application as required.

Therefore, the inventions related to Claims 1 through 7 of the present application could have been easily invented by a person skilled in the art, based on the inventions described in Cited Literature 1 through 5.

List of Cited Literature

1. Japanese Unexamined Patent Application Publication H11-261021

2. Japanese Unexamined Patent Application Publication 2000-082803
3. Japanese Unexamined Patent Application Publication H11-186524
4. Japanese Unexamined Patent Application Publication H11-307740
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STATEMENT UNDER 37 C.F.R. § 1.97(e)

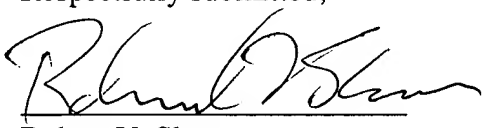
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The undersigned hereby states, upon information and belief:

That each item of information contained in the Information Disclosure Statement filed concurrently herewith was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of said Information Disclosure Statement.

Respectfully submitted,



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Substitute for Form 1449 A & B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/817,233
Confirmation Number	8072
Filing Date	March 27, 2001
First Named Inventor	Ryo KUBOTO
Art Unit	2823
Examiner Name	Hsien Ming LEE
Attorney Docket Number	Q62494

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number	Document Number: Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US			
		US			
		US			
		US			
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		US			
		US			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]	Foreign Patent Document: Number[4]	Foreign Patent Document: Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation[6]
		JP	H11-261031		09-24-1999		No
		JP	2000-82803	A	05-21-2000		No

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kind Codes of USPTO Patent Documents at www.uspto.gov, MPEP 901.04 or in the comment box of this document. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to indicate here if English language Translation is attached.